Claims

1. A method for forming a micro-mechanical component in a semiconductor wafer comprising a membrane layer supported on a handle layer with a buried insulating layer disposed between the membrane layer and the handle layer, the micro-mechanical component being formed in the membrane layer, and a communicating opening extending through the handle layer and the buried insulating layer exposing the micro-mechanical component, the method comprising the steps of:

forming at least one trench extending through the membrane layer for defining the micro-mechanical component therein, each trench exposing a portion of the buried insulating layer bridging the trench,

applying a support layer to each bridging portion of the buried insulating layer, the support layer extending across each trench, and being applied to each bridging portion of the buried insulating layer prior to the bridging portion being exposed by the communicating opening through the handle layer for supporting the bridging portion for preventing rupturing of the buried insulating layer when the buried insulating layer is exposed by the communicating opening through the handle layer.

2. A method as claimed in Claim 1 in which the support layer is applied to each bridging portion of the buried insulating layer by back filling the corresponding trench formed in the membrane layer with material for forming the support layer.

3. A method as claimed in Claim 1 in which the support layer is applied to the surface of the micro-mechanical component in a plane parallel to the plane of the exposed surface of the membrane layer for preventing bowing of the micro-mechanical component when the communicating opening has been formed in the handle layer, and prior to the buried insulating layer adjacent the micro-mechanical component exposed by the communicating opening being removed.

4. A method as claimed in Claim 1 in which the support layer is applied to the entire exposed surface of the micro-mechanical component.

5. A method as claimed in Claim 1 in which the support layer is applied to the exposed surface of the membrane layer adjacent the micro-mechanical component.

6. A method as claimed in Claim 1 in which the support layer is applied to the entire exposed surface of the membrane layer.

7. A method as claimed in Claim 1 in which the support layer is deposited.

8. A method as claimed in Claim 1 in which the support layer is an oxide support layer.

9. A method as claimed in Claim 8 in which the depth of the oxide support layer is in the range of 0.4μm to 2μm.

10. A method as claimed in Claim 9 in which the depth of the oxide support layer is in the order of 1μm.

11. A method as claimed in Claim 1 in which the support layer is of photo-resist material.

12. A method as claimed in Claim 11 in which the depth of the photo-resist support layer is in the range of 1μm to 10μm.

13. A method as claimed in Claim 12 in which the depth of the photo-resist support layer is in the order of 5μm.

14. A method as claimed in Claim 1 in which the support layer comprises a first support layer, and a second support layer applied over the first support layer.

15. A method as claimed in Claim 14 in which the first support layer is an oxide layer.

16. A method as claimed in Claim 15 in which the oxide of the first support layer is deposited.

17. A method as claimed in Claim 16 in which the first support layer of oxide is of

depth in the range of 0.4μm to 1.5μm.

18. A method as claimed in Claim 17 in which the first support layer of oxide is of depth in the order of 1μm.

19. A method as claimed in Claim 14 in which the second support layer is a silicon based layer.

20. A method as claimed in Claim 19 in which the second support layer is a deposited layer.

21. A method as claimed in Claim 19 in which the second support layer is a polysilicon layer.

22. A method as claimed in Claim 21 in which the second support layer of polysilicon is of depth in the range of 1μm to 10μm.

23. A method as claimed in Claim 22 in which the second support layer of polysilicon is of depth in the order of 4μm.

24. A method as claimed in Claim 19 in which the second support layer comprises a silicon wafer bonded to the first support layer.

25. A method as claimed in Claim 24 in which the second support layer in the form of a silicon wafer, while it is acting as a support layer is of depth in the range of 5μm to 100μm.

26. A method as claimed in Claim 25 in which the second support layer in the form of a silicon wafer, while it is acting as a support layer is of depth in the order of 20μm.

27. A method as claimed in Claim 14 in which an access opening is etched through the second support layer for providing access to the micro-mechanical component through the second support layer, and the portion of the first support layer adjacent the micro-mechanical component is removed through the access opening.

28. A method as claimed in Claim 1 in which the portion of the buried insulating layer exposed by the communicating opening and the support layer are removed when the communicating opening has been formed in the handle layer.

29. A method as claimed in Claim 28 in which the portion of the buried insulating layer exposed by the communicating opening is removed before the support layer is removed.

30. A method as claimed in Claim 28 in which the support layer and the portion of the buried insulating layer exposed by the communicating opening are simultaneously removed.

31. A method as claimed in Claim 1 in which the micro-mechanical component is a micro-mirror supported in the membrane layer by a pair of tethers located on opposite sides of the micro-mirror for defining a pivot access about which the micro-mirror is tiltable.

32. A method as claimed in Claim 1 in which the depth of the membrane layer is in the range of 2μm to 30μm.

33. A method as claimed in Claim 1 in which the depth of the membrane layer is in the order of 3μm.

34. A method as claimed in Claim 1 in which the buried insulating layer is of depth in the range of 0.2μm to 1μm.

35. A method as claimed in Claim 1 in which the buried insulating layer is in the order of 0.4μm.

36. A semiconductor wafer comprising:

a handle layer,

a membrane layer supported on the handle layer,

a buried insulating layer disposed between the membrane layer and the handle layer, and

a micro-mechanical component formed in the membrane layer and supported

therein, the semiconductor wafer being formed according to the method as claimed in Claim 1.

37. A semiconductor wafer as claimed in Claim 36 in which a communicating opening extends through the handle layer to the micro-mechanical component.

38. A semiconductor wafer comprising:

a handle layer,

a membrane layer supported on the handle layer,

a buried insulating layer disposed between the membrane layer and the handle layer,

a micro-mechanical component formed in the membrane layer by at least one trench extending through the membrane layer, and supported therein, and

a communicating opening extending through the handle layer and the buried insulating layer to the micro-mechanical component, wherein

prior to forming the communicating opening a support layer is applied to each bridging portion of the buried insulating layer, the support layer extending across each trench, and being applied to each bridging portion of the buried insulating layer prior to the bridging portion being exposed by the communicating opening through the handle layer for supporting the bridging portion for preventing rupturing of the buried insulating layer when the buried insulating layer is exposed by the communicating opening through the handle layer, the support layer being removed subsequently.